40 GHz Hot-Via Flip-Chip Interconnects

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Abstract — **A hot-via flip-chip interconnect for the 40 GHz band is presented. The chip in-out cell includes on-wafer probing pads and is minimized with regard to size. An optimized design shows excellent performance with 10 GHz of bandwidth and –40 dB isolation. This demonstrates the potential of the hot-via approach in mm-wave applications.**

I. Motivation

The flip-chip approach (e.g. [1]) is known to provide good broadband properties even in the mm-wave frequency range. However, in order to achieve optimum performance, it requires coplanar chips. Since most existing chip designs are of the microstrip type, one has been thinking of modified flip-chip approaches, which are better adapted to the microstrip geometry. This is of particular importance for power chips.

Most promising in this regard is the so-called hot-via solution [2]: the chip is mounted by means of bumps on the carrier substrate, yet not flipped but in upright position. Since the contact region is on the backside of the chip, the metalization on this side has to be structured as well, which increases chip processing complexity. The signal line on the chip is connected to the backside and the bump interconnect using a via-hole, the "hot via". Several variants of this mounting scheme have been proposed (see [3,4,5]).

Beside its compatibility with microstrip designs, there are more benefits of this approach: first, the chip can be optically inspected after mounting, which is in line with common assembly processes. The second advantage comes from the backside metalization of the microstrip chip, which acts as a shielding against the structures underneath the chip. Thus, detuning effects are eliminated.

On the other hand, the interconnect is electrically larger than the corresponding conventional flip-chip one. This degrades high-frequency performance, but to which extent? Though one finds simulations on the hot-via interconnect in the literature, an experimental validation in the mm-wave range is still missing. This open question motivated the work presented in the following. Its purpose is to explore the frequency limits of the hot-via approach under realistic conditions. As an example of great practical relevance, a 38 GHz interconnect was chosen.

II. The Hot-Via Interconnect

Fig. 1 presents the interconnect. A standard 100 µm thick GaAs chip with a 50 Ω microstrip line is used. The signal strip is connected to a pad at the backside of the chip. The chip is mounted on the motherboard in an upright position. Bumps connect the pad structure on the chip backside with its counterpart on the motherboard. There, we use coplanar waveguide (CPW) as transmission-line element.

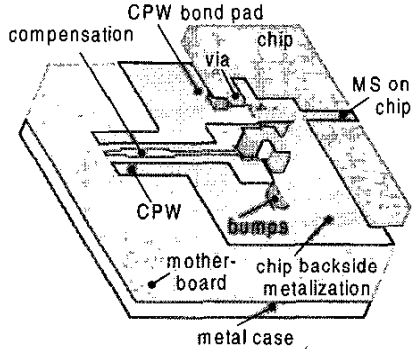

Fig. 1 The hot-via flip-chip interconnect (bumps not to scale).

After bonding the bumps are about 30 µm high with a diameter of 75 µm. The via on the chip is the standard via available in the UMS process. As can be seen from Fig. 1, on-wafer probing pads are added on the chip. Their purpose is to allow automated on-wafer characterization of the chip prior to mounting (in this case, a non-conducting substrate has to be placed between chip and measurement chuck because otherwise the in-out cell would be short-circuited from the backside).

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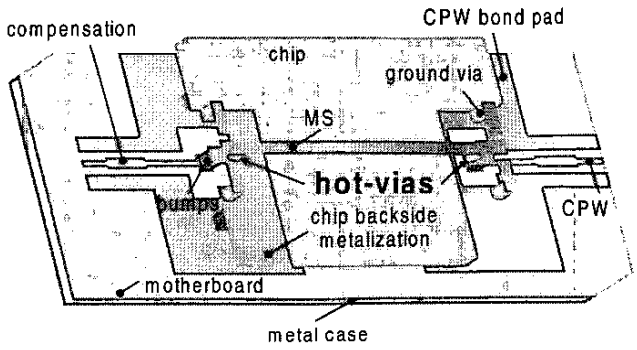

Fig. 2 (a): The back-to-back structure including 2 hot-via transitions and a microstrip thru-line on the chip. Here, the motherboard ground metalization between the two CPW bond pads is not connected.

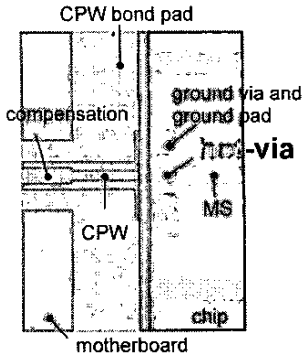

Fig. 2(b): Photography of a single hot-via transition with chip mounted.

Optimization was performed by means of 3D electromagnetic simulation using the FBH finite-difference frequency-domain code. In a first step, the layout of the interconnect is optimized. Parameters are the various pad and slot dimensions. The goal is to achieve low reflection while minimizing the area of the in-out cell on the GaAs chip. Constraints are the layout constraints for the chip process, particularly those of the backside, and the required pad size and spacing for the automatic on-wafer probing. Altogether, this does neither allow many degrees of freedom nor a significant downscaling of the dimensions. Also, the ground pads for on-wafer probing represent a capacitive load in the mounted case, which deteriorates reflection behavior of the interconnect significantly. Therefore, in a second step, a compensation structure on the motherboard is implemented, which is designed to reduce reflections in a band centered around 38 GHz.

III. The Realized Structure

For measurement verification, a back-to-back test structure was realized. It consists of a passive GaAs microstrip chip with thru-line connections (a 2470 µm long homogeneous line) and opposite stubs, which allow measurement of isolation properties. The chip is mounted onto a motherboard using the hot-via interconnect described above. Fig. 2 illustrates the thru-line structure. It is measured on-wafer between the CPW lines on the motherboard.

Since the motherboard backside is metalized, it supports a parallel-plate line (PPL) mode. Using a continuous ground plane on top of the motherboard below the chip gives rise to an additional PPL mode, which propagates in the air gap between chip backside and ground metalization on the motherboard.

In order to estimate how the excited PPL modes influence the overall behavior, we investigated two designs with different layout of the CPW ground plane on top of the motherboard. In one case the ground metalization underneath the chip is removed (1870 µm gap width, see Fig. 2(a)), in the other both bond-pad areas are connected by a continuous ground. These two cases will be referred to as "ground connected" and "ground disconnected" in the following.

IV. Results

Fig. 3 presents the results of the back-to-back thru-line with uncompensated interconnects, which was included in the design for comparison. One observes good agreement between the values predicted by simulation and measurements. The reflections are in the order of –10 dB for the back-to-back case, which is not very high but above the specified value of –20 dB. The differences between connected and disconnected ground on the motherboard are visible but not significant.

In Fig. 4, the results for the compensated structure and connected ground are plotted. Fig. 5 adds the corresponding data for the case of a disconnected ground. Each figure displays three curves. They refer to the values predicted by em simulation for the realized geometry and the measurements. The third curve labelled "optimization" is included to estimate, which further improvement can be expected after a redesign.

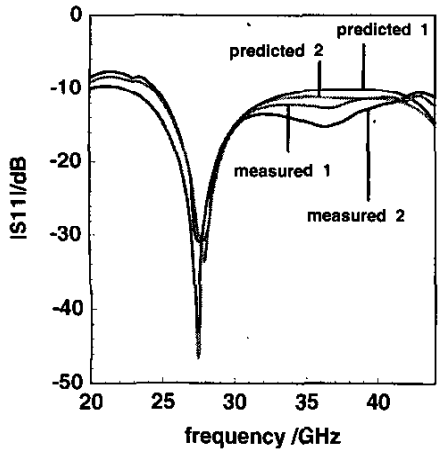

Fig. 3 Reflections at the uncompensated hot-via back-to-back-structure against frequency: predictions by em simulation and measurements (thru-line structure according to Fig. 2(a).
1 : ground connected.
2 : ground disconnected.

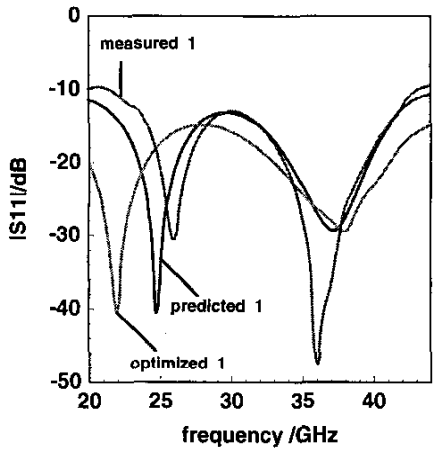

Fig. 4 Reflection coefficient of the compensated hot-via back-to-back-structure with ground connected as a function of frequency (thru-line structure, see Fig. 2(a).with continuous ground plane); predictions by em simulation, measured data and redesign (simulations).

Quantitatively, measured return loss for the compensated case remains beyond 20 dB within more than 5 GHz around 38 GHz. This means a level of 25 dB for the single interconnect, which fully meets the usual specs. As indicated by the "optimized" curve, a redesign can further increase the bandwidth to about 10 GHz. These results document feasibility of the hot-via interconnect for the 40 GHz range and indicate that even higher frequencies appear to be possible, at the expense of bandwidth, of course. The measured insertion loss, corrected by line attenuation, is below 0.5 dB per transition at 38 GHz.

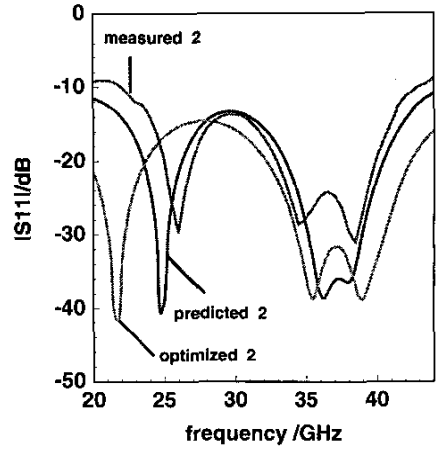

Fig. 5 Reflection coefficient of the compensated hot-via back-to-back-structure as a function of frequency – data of Fig. 4 for the case with ground disconnected.

The differences between the disconnected and connected ground become obvious only in the low reflection range around 38 GHz. In order to further explore these effects, the excitation of the parasitic PPL modes is studied. Fig. 6 presents the simulated transmission coefficients from CPW and microstrip to the various PPL modes at a single interconnect, for the case of the connected ground. Here, PPL modes exist in the conductor-backed CPW section on the motherboard (PPL1), in the motherboard below the chip (PPL2), and in the air gap between motherboard ground and chip backside metalization (PPL3).

As can be seen from Fig. 6, the highest transmission occurs from the microstrip mode into PPL1, i.e., the PPL mode in the CB-CPW section, and from the CPW mode into the PPL2 mode, i.e., the PPL mode within the motherboard in the chip section. All other transmission coefficients are lower, in the –20...-30 dB range. Comparing the results of Figs. 4 and 5, one finds that the usable bandwidth (i.e., the frequency band with reflections lower than –20 dB) is quite similar though the curves show a different behavior in the passband. One can state that PPL effects are visible but low enough to corrupt return loss characteristics in the critical level where reflections exceed 20 dB.

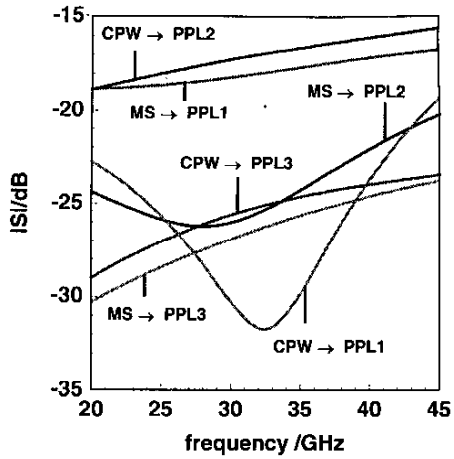

Fig. 6 Calculated transmission coefficients from CPW and microstrip mode (CPW, MS) into the PPL modes as a function of frequency; structure with connected ground metalization on motherboard.

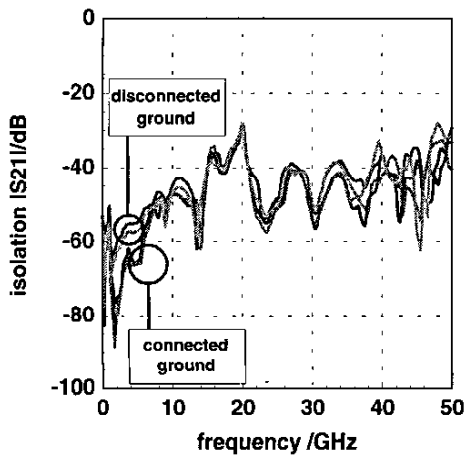

Fig. 7 Measured transmission between two microstrip shorts on the chip (1000 µm distance) against frequency; back-to-back environment, data of 4 mounted chips (2 with connected, 2 with disconnected ground on top of the substrate).

Regarding crosstalk, the structure most suitable to detect such effects is a set-up with two opposite stubs (shorted or open-ended) on the chip. Ideally, transmission should be zero, the resulting finite value is solely due to crosstalk between the ports and allows reliable determination of port isolation. Therefore, we included two shorted microstrip stub lines on the chip in the back-to-back-structure with a distance of 1000 µm. Fig. 7 presents the corresponding measurements. As can be seen, isolation is better than –30 dB in the entire frequency range up to 50 GHz and around –40 dB in most parts of the band. This is in the order of the on-chip coupling. Hence, the mounting scheme does not contribute significantly to crosstalk and isolation as is desirable.

V. Conclusions

After suitable optimization, the hot-via flip-chip interconnect exhibits excellent performance within a bandwidth of 5...10 GHz at 40 GHz: an insertion loss in the order of 0.5 dB is obtained, the return loss exceeds 20 dB for a back-to-back structure, and isolation is larger than 30 dB in the entire frequency range up to 50 GHz. This demonstrates the potential of this approach for the mm-wave range. Frequencies higher than 40 GHz, e.g., around 60 GHz or even 77 GHz, appear to be feasible when sacrificing bandwidth.

Acknowledgement

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